Attorney Docket: 0325.00368

IN RE APPLICATION OF: Steven P. Larky et al.

SERIAL NO.: 09/631,427

TITLE: ANALOG SIGNAL VERIFICATION USING DIGITAL SIGNATURES

FILED: August 3, 2000

EXAMINER: Day, H.

ART UNIT: 2128

RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)

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Total Claims	20 minus	20 =	0 x $ 50.00	$ 0.00
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Multiple Dependent Claim First Added			+ $360.00	$0.00

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By: Mary Donna Berkley
Mary Donna Berkley

Our Docket No.: 0325.00368

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Steven P. Larkey et al.		
Application No.:	09/631,427	Examiner:	Day, H.
Filed:	August 3, 2000	Art Group:	2128
For:	ANALOG SIGNAL VERIFICATION USING DIGITAL SIGNATURES		

CERTIFICATE OF MAILING

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 10, 2005.

By: Mary Donna Berkley
Mary Donna Berkley

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b)(2). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-11 and 21-29 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-11 and 21-29.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on November 5, 2004. On January 5, 2005, Appellants filed a Response After Final that did not amend the claims and requested reconsideration. On February 16, 2005, the Examiner issued an Advisory indicating that the rejections were maintained. On March 15, 2005, Appellants filed a Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A first embodiment of the present invention (as represented by claim 1) generally concerns a method 100 for verification. The method generally comprises the step of (A) generating

108 one or more analog signals ANALOG. The one or more analog signals may be utilized by the analog design. Generation of the analog signals is generally described in the specification on page 4, lines 18-21. Another step of the method may be (B) generating 110 one or more source signals AN_D by adding a digital signature to each of the analog signals. Creation and addition of the digital signatures to the analog signals is generally described in the specification starting on page 4, line 21 through page 5, line 8 of the specification. Examples of digital signatures are provided on page 8, lines 8-13. Another step of the method may include (C) modeling 104 an analog design using the source signals in place of the analog signals for verifying connectivity. Modeling with the source signals is generally described in the specification from page 9, line 3 through page 11, line 9.

A second embodiment of the present invention (as represented by claim 9) generally concerns a method 200 for testing a model of an analog device. The method may include a step (A) for generating 206 one or more attributed signals AN_D each (i) having a unique digital signature and (ii) presented by a source block within the model of the analog device. Generation of the attributed signals is generally described in the specification on page 4, lines 18-21. Examples of digital signature attributes are provided on page 8, lines 8-13. The method may include a step for (B) verifying connectivity 212 of the attributed signals to a destination block within the model of the analog device by verifying 210 reception of the unique digital signatures associated with each of the attributed signals at the destination block. Verification of the connectivity is generally described in the specification on page 9, line 3 through page 11, line 9.

A third embodiment of the present invention (as represented by claim 23) generally concerns a system 100. The system may include (i) a source 102 for a plurality of signals DIGITAL and AN_D and (ii) a simulator 104 connected to the source. At least one of the signals AN_D may represent an analog signal ANALOG having a digital signature. Generation of the analog signals is generally described in the specification on page 4, lines 18-21. Creation and addition of the digital signatures to the analog signals is generally described in the specification starting on page 4, line 21 through page 5, line 8 of the specification. Examples of digital signatures are provided on page 8, lines 8-13. The simulator may be configured to (i) simulate an analog design, (ii) receive the signals and (iii) verify a connectivity of the analog signal in the analog design using the digital signature. Simulating the analog design is generally described in the specification from page 9, line 3 through page 11, line 9. Reception of the signals is illustrated in FIG. 1. Verification of the connectivity is generally described in the specification on page 9, line 3 through page 11, line 9.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first issue is whether claims 1-11, 21, 22, 25 and 26 are patentable under 35 U.S.C. §112, first paragraph, enablement.

The second issue is whether claims 1-11 and 21-29 are patentable under 35 U.S.C. §102(b) over "A Current Integrator for BIST of Mixed-Signal IC's" by Tabatabaei et al. (hereafter Tabatabaei).

VII. ARGUMENTS

A. 35 U.S.C. §112

1. Claims 1-11, 21, 22, 25 and 26 are fully compliant with 35 U.S.C. §112, first paragraph, enablement.

The Examiner fails to provide evidence or reasoning why one of ordinary skill in the art would be unable to make and/or use the invention without undue experimentation. The Examiner merely states that "without undue experimentation, it is unclear for one skilled in the art how to generate" the various claimed signals by "adding a digital signature".[1] Regarding an enablement rejection, the Manual of Patent Examining Procedures[2] (MPEP) §2164.04 states:

> In order to make a rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1990). ... [T]he examiner should specifically identify what information is missing and **why** one skilled in the art could not supply the information without undue experimentation. ... However, **specific technical reasons are always required.** (Emphasis added)

The assertions by the Examiner that undue experimentation would be necessary appear to be merely a conclusory statement lacking the required support. No explanation why or specific technical reasons were provided as required by MPEP §2164.04. Therefore, the initial burden for the 35 U.S.C. §112, first paragraph, enablement rejection has not been meet.

The Examiner provided a list of things that one of ordinary skill in the art would allegedly have to consider to add a digital signature to an analog signal in the Advisory.[3] However,

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[1] Office Action Final, November 5, 2004, page 3, paragraphs 5-1, 5-2 and 5-3.

[2] MPEP, Eighth Edition, Rev. 2, May 2004.

[3] Advisory, February 16, 2005, last page.

once again, the Examiner does not provide any evidence or convincing line of reasoning why the items in the list would mean that one of ordinary skill in the art would be unable to practice the invention without undue experimentation. Therefore, the initial burden for the 35 U.S.C. §112, first paragraph, enablement rejection has not been meet.

Furthermore, the specification provides several examples of the digital signatures on page 8, lines 8-13. In one example, the digital signature may be (iii) a series of pulses of known width. One of ordinary skill in the art would appear to understand how to add a series of pulses to an analog signal. For example, adding horizontal and vertical sync pulses to an analog video signal appears to be within the capabilities of those of ordinary skill. As such, the claims are fully compliant with 35 U.S.C. §112, first paragraph, enablement, and the rejection should be reversed.

B. 35 U.S.C. §102

The Federal Circuit has stated that "[t]o anticipate, **every element and limitation** of the claimed invention must be found in a single prior art reference, **arranged as in the claim.**"[4] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[5]

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[4] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[5] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[6]

1. Claims 1 and 2 are fully patentable over Tabatabaei

Claim 1 provides a step for generating one or more source signals by adding a digital signature to each of one or more analog signals. Instead of giving the claim language its plain meaning, the Examiner provided an interpreted meaning. Interpretation of the claims is discussed in MPEP §2111:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation **consistent with the specification.**" *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664m 1667 (Fed. Cir. 2000) . . . The broadest reasonable interpretation of the claims must also be **consistent with the interpretation that those skilled in the art would reach**. *In re Cortright*, 165 F.3d 1353, 1359, 48 USPQ2d 1464, 1468 (Fed. Cir. 1999). (Emphasis added)

Furthermore, MPEP §2111.01 states:

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. ... This means that the words of the **claim must be given their plain meaning** unless applicant has provided a clear definition in the specification. ... The broadest reasonable interpretation of the claims **must be consistent with the interpretation that those skilled in the art would reach**. (Emphasis added)

In contrast, the Examiner fails to interpret the claim (i) consistent with the specification, (ii) consistent with an interpretation one of ordinary skill in the art would reach and (iii) consistent with the plain meaning. In particular, the Examiner interprets "adding a digital signature to an analog

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[6] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

signal" to be the same as "generating a digital signal proportional to average supply current".[7] However, the Examiner provides no evidence or convincing line of reasoning that "generating a digital signature proportional to average supply current" is (i) consistent with the specification and (ii) would be reached by one of ordinary skill in the art. As such, the Examiner's interpretation appears to be improper.

Furthermore, the claim interpretation provided by the Examiner appears to go well beyond the plain meaning of the claim language by completely eliminating the "adding" operation. The elimination of the "adding" operation is in conflict with the "add" portion of block 110 in FIG. 1 and the "Add digital signature" block 206 in FIG. 2. Therefore, the Examiner's interpretation appears to be improper and should be ignored.

Claim 1 provides a step for generating one or more source signals by adding a digital signature to each of one or more analog signals. In contrast, Tabatabaei appears to be silent regarding adding digital signatures to analog signals. Furthermore, Tabatabaei does not appear to discuss adding a signal "n-bit N" (asserted similar to the claimed digital signature[8]) to a signal I_{DD} (asserted similar to the claimed analog signal[9]) or any other analog signal. Therefore, Tabatabaei does not appear to disclose or suggest a step for generating one or more source signals by adding a digital signature to each of one or more analog signals as presently claimed.

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[7] Office Action Final, November 5, 2004, page 3, paragraph 6.

[8] Office Action Final, November 5, 2004, page 4, paragraph 8-1.

[9] Office Action Final, November 5, 2004, page 4, paragraph 8-1.

Furthermore, the Examiner fails to show that Tabatabaei allegedly anticipates the claimed step. In particular, the Examiner merely argues "n-bit N, Figure 1".[10] The words "n-bit N" do not appear to anticipate a step for generating one or more source signals by adding a digital signature to each of one or more analog signals as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

Claim 1 further provides a step for modeling an analog design using source signals having digital signatures in place of the analog signals for verifying connectivity. Despite the assertion by the Examiner,[11] the first paragraph in section 3 of Tabatabaei appears to be silent regarding both (i) modeling an analog design using source signals having digital signatures **in place of** analog signals and (ii) verifying connectivity. Therefore, Tabatabaei does not appear to disclose or suggest a step for modeling an analog design using source signals having digital signatures in place of analog signals for verifying connectivity as presently claimed.

Furthermore, the Examiner merely argues "discard this circuit, section 3, paragraph 1".[12] The phrase "discard this circuit" does not appear to anticipate a step for modeling an analog design using source signals having digital signatures in place of analog signals for verifying connectivity as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

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[10] Office Action Final, November 5, 2004, page 4, paragraph 8-1.

[11] Office Action Final, November 5, 2004, page 4, paragraph 8-1.

[12] Office Action Final, November 5, 2004, page 4, paragraph 8-1.

Assuming, *arguendo*, that the Examiner's interpretation of the "adding" claim language is correct (for which Appellants' representative does not agree), the Examiner still fails to establish that Tabatabaei discusses modeling a circuit with the signal "n-bit N" (asserted similar to the claimed digital signature) in place of the signal I_{DD} (asserted similar to the claimed analog signal) as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the rejection for claim 1 should be reversed.

2. Claim 9 is fully patentable over Tabatabaei

Claim 9 provides a step for generating one or more attributed signals each having a unique digital signature. Instead of giving the claim language its plain meaning, the Examiner provided an interpreted meaning. Interpretation of the claims is discussed in MPEP §2111:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation **consistent with the specification.**" *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664m 1667 (Fed. Cir. 2000) . . . The broadest reasonable interpretation of the claims must also be **consistent with the interpretation that those skilled in the art would reach**. *In re Cortright*, 165 F.3d 1353, 1359, 48 USPQ2d 1464, 1468 (Fed. Cir. 1999). (Emphasis added)

Furthermore, MPEP §2111.01 states:

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. ... This means that the words of the **claim must be given their plain meaning** unless applicant has provided a clear definition in the specification. ... The broadest reasonable interpretation of the claims **must be consistent with the interpretation that those skilled in the art would reach**. (Emphasis added)

In contrast, the Examiner fails to interpret the claim (i) consistent with the specification, (ii) consistent with an interpretation one of ordinary skill in the art would reach and (iii) consistent with

the plain meaning. In particular, the Examiner interprets "generating one or more attributed signals each having a unique digital signature" to be the same as "generating a digital signal proportional to average supply current".[13] However, the Examiner provides no evidence or convincing line of reasoning that "generating a digital signature proportional to average supply current" is (i) consistent with the specification and (ii) would be reached by one of ordinary skill in the art. As such, the Examiner's interpretation appears to be improper.

Furthermore, the claim interpretation provided by the Examiner appears to go well beyond the plain meaning of the claim language by completely eliminating the "having a digital signature" limitation as used in the claim. The elimination of the "having a digital signature" limitation is in conflict with the "add" portion of block 110 in FIG. 1 and the "Add digital signature" block 206 in FIG. 2. Therefore, the Examiner's interpretation appears to be improper and should be ignored.

Regarding the step for generating one or more attributed signals each having a unique digital signature, Tabatabaei appears to be silent regarding any signal having unique digital signatures. Furthermore, Tabatabaei does not appear discuss a signal "n-bit N" (asserted similar to the claimed attributed signal[14]) having a unique digital signature. Therefore, Tabatabaei does not appear to disclose or suggest a step for generating one or more attributed signals each having a unique digital signature as presently claimed.

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[13] Office Action Final, November 5, 2004, page 3, paragraph 6.

[14] Office Action Final, November 5, 2004, page 6, paragraph 8-9.

Furthermore, the Examiner merely argues "n-bit N, Figure 1".[15] The words "n-bit N" do not appear to anticipate a step for generating one or more attributed signals each having a unique digital signature as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

Claim 9 further provides a step for verifying connectivity of the attributed signals from a source block to a destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals at the destination block. In contrast, Tabatabaei appears to be silent regarding both (i) verification of connectivity between blocks and (ii) verification for reception of a digital signature at a destination block. Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying connectivity of attributed signals from a source block to a destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals at the destination block as presently claimed.

Furthermore, the Examiner merely argues "discard this circuit, section 3, paragraph 1".[16] The phrase "discard this circuit" does not appear to anticipate a step for verifying connectivity of the attributed signals from a source block to a destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals at the destination block as presently claimed. As such, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

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[15] Office Action Final, November 5, 2004, page 6, paragraph 8-9.

[16] Office Action Final, November 5, 2004, page 6, paragraph 8-9.

Furthermore, the argument by the Examiner that Tabatabaei discusses "discarding this [faulty] circuit"[17] does not appear to have any relevance to the claimed step of verifying connectivity of attributed signals to a destination block within a model to an analog device. The full sentence cited in section 3, paragraph 1 of Tabatabaei reads:

> If the average current measured for a faulty circuit is 20 uA, even with 25% error for this value (the actual average current could be 25 uA < 50 uA), the decision to discard this circuit is correct.

Tabatabaei appears to contemplate discarding a silicon chip having a faulty circuit rather than discarding a model of the circuit. If there was no connectivity in the model, then the average current measured would appear to be zero current (e.g., zero uA). Therefore, *prima facie* anticipation has not been established for lack of evidence that Tabatabaei discloses or suggest all of the claim limitations. As such, the rejection for claim 9 should be reversed.

3. Claim 23 is fully patentable over Tabatabaei

Claim 23 provides a source for a plurality of signals and a simulator connected to the source. Despite the assertion by the Examiner,[18] Tabatabaei appears to be silent regarding a simulator connected to a Built-In Current Integrator block (asserted similar to the claimed source) for a signal n-bit N (asserted similar to the claimed digital signature). Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests the claimed structure.

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[17] Office Action Final, November 5, 2004, page 6, paragraph 8-9.

[18] Office Action Final, November 5, 2004, page 7, paragraph 8-14.

Claim 23 further provides that at least one of the signals represents an analog signal having a digital signature. In contrast, Tabatabaei appears to be silent regarding any analog signal having a digital signature. Therefore, Tabatabaei does not appear to disclose or suggest that at least one signal represents an analog signal having a digital signature as presently claimed. Furthermore, the Examiner makes no argument for claim 23 that Tabatabaei mentions an analog signal having a digital signature as presently claimed.[19] Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

Furthermore, the Examiner merely argues "I_{DD} and n-bit N, Figure 1".[20] The phrase "I_{DD} and n-bit N" does not appear to anticipate that at least one signal represents an analog signal having a digital signature as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

Claim 23 further provides that the simulator is configured to verify a connectivity of an analog signal in an analog design using a digital signature. Despite the assertion by the Examiner,[21] Tabatabaei appears to be silent regarding a simulator verifying connectivity of an analog signal in an analog design using a digital signature as presently claimed. Merely pointing out that Tabatabaei mentions a simulator does not appear to prove use of a digital signature by the simulator to verify a connectivity of an analog signal.

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[19] The Examiner's claim interpretation is for dependent claim 25, not independent claim 23.

[20] Office Action Final, November 5, 2004, page 7, paragraph 8-14.

[21] Office Action Final, November 5, 2004, page 7, paragraph 8-14.

Furthermore, the Examiner merely argues "simulator, section 3, paragraph 1"[22]. The word "simulator" does not appear to anticipate a simulator configured to verify a connectivity of an analog signal in an analog design using a digital signature as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection for claim 23 should be reversed.

4. Claim 3 is fully patentable over Tabatabaei

Claim 3 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 3.

Claim 3 further provides that each digital signature corresponds to a type of the analog signals having a predetermined parameter. Despite the assertion by the Examiner,[23] the Abstract of Tabatabaei appears to be silent regarding different types of analog signals having predetermined parameters. Therefore, Tabatabaei does not appear to disclose or suggest that each digital signature corresponds to a type of analog signal having a predetermined parameter as presently claimed.

Furthermore, the Examiner merely argues "average supply current, abstract"[24]. The phrase "average supply current" does not appear to anticipate each digital signature corresponding

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[22] Office Action Final, November 5, 2004, page 7, paragraph 8-14.

[23] Office Action Final, November 5, 2004, page 5, paragraph 8-3.

[24] Office Action Final, November 5, 2004, page 5, paragraph 8-3.

to a type of analog signal having a predetermined parameter as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 3 should be reversed.

5. Claim 4 is fully patentable over Tabatabaei

Claim 4 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 4.

Claim 4 further provides that each of the digital signatures comprises a unique pulse width. Despite the assertion by the Examiner,[25] Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature) having unique pulse widths as presently claimed. Therefore, Tabatabaei does not appear to disclose or suggest that each of one or more digital signatures comprises a unique pulse width as presently claimed.

Furthermore, the Examiner merely argues "n-bit N, Figure 1".[26] The words "n-bit N" do not appear to anticipate each of one or more of digital signatures comprising a unique pulse width as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 4 should be reversed.

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[25] Office Action Final, November 5, 2004, page 5, paragraph 8-4.

[26] Office Action Final, November 5, 2004, page 5, paragraph 8-4.

6. Claim 5 is fully patentable over Tabatabaei

Claim 5 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 5.

Claim 5 further provides a step for performing verification of an analog design. Despite the assertion by the Examiner,[27] the first paragraph of section 3 in Tabatabaei appears to be silent regarding circuit verification. Therefore, Tabatabaei does not appear to disclose or suggest a step for performing verification of an analog design as presently claimed.

Furthermore, the Examiner merely argues "discard this circuit, section 3, paragraph 1".[28] The phrase "discard this circuit" does not appear to anticipate a step for performing verification of an analog design as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 5 should be reversed.

7. Claim 6 is fully patentable over Tabatabaei

Claim 6 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 6.

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[27] Office Action Final, November 5, 2004, page 5, paragraph 8-5.

[28] Office Action Final, November 5, 2004, page 5, paragraph 8-5.

Claim 6 further provides a step for verifying a connectivity of analog signals through an analog design. Despite the assertion by the Examiner,[29] the first paragraph of section 3 in Tabatabaei appears to be silent regarding verifying connectivity for an analog signal through a circuit design. Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying a connectivity of analog signals through an analog design as presently claimed.

Furthermore, the Examiner merely argues, "discard this circuit, section 3, paragraph 1".[30] The phrase "discard this circuit" does not appear to anticipate a step for performing verification of an analog design as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 6 should be reversed.

8. Claim 7 is fully patentable over Tabatabaei

Claim 7 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 7.

Claim 7 further provides a step for verifying a model of an analog block within an analog design configured to receive at least a particular one of the analog signals. Despite the assertion by the Examiner,[31] Tabatabaei appears to be silent regarding a model of an analog block

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[29] Office Action Final, November 5, 2004, page 5, paragraph 8-6.

[30] Office Action Final, November 5, 2004, page 5, paragraph 8-6.

[31] Office Action Final, November 5, 2004, page 5, paragraph 8-7.

receiving a signal SIN2 (asserted similar to the claimed at least one particular analog signal). Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying a model of an analog block within an analog design configured to receive at least a particular one of the analog signals as presently claimed.

Claim 7 further provides (from claim 1) a step of generating one or more source signals by adding a digital signature to each of the analog signals. In contrast, Tabatabaei appears to be silent regarding adding a digital signature to the signal SIN2 (asserted similar to the claimed at least a particular one of the analog signals). Therefore, Tabatabaei does not appear to disclose or suggest a step of generating one or more source signals by adding a digital signature to each of the analog signals as presently claimed. Furthermore, the Examiner makes no argument that Tabatabaei mentions adding a digital signature to the signal SIN2. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, claim 7 is fully patentable over the cited reference and the rejection should be reversed.

9. Claim 8 is fully patentable over Tabatabaei

Claim 8 depends from claim 7 and thus contains all of the limitations of claim 7. Consequently, the arguments presented above in support of the patentability of claim 7 are incorporated hereunder in support of claim 8.

Claim 8 further provides a step for verifying an output signal of the analog block (from claim 7) for the digital signature associated with the particular one of the analog signals. In

contrast, the Examiner appears to be asserting that the signal SIN2 is both the input[32] and output[33] of some unidentified analog block. Since one of ordinary skill in the art would not consider a single signal SIN2 to simultaneously anticipate two different claimed signals, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, claim 8 is fully patentable over the cited reference and the rejection should be reversed.

10. Claim 10 is fully patentable over Tabatabaei

Claim 10 depends from claim 9 and thus contains all of the limitations of claim 9. Consequently, the arguments presented above in support of the patentability of claim 9 are incorporated hereunder in support of claim 10.

Claim 10 further provides a step of disabling processing of a particular one of a plurality of attributed signals if a particular signal is not verified at a destination block. Despite the assertion by the Examiner,[34] the first paragraph in section 3 of Tabatabaei appears to be silent regarding disabling processing of a particular one of a plurality of attributed signals if a particular signal is not verified at a destination block. Therefore, Tabatabaei does not appear to disclose or suggest a step of disabling processing of a particular one of a plurality of attributed signals if a particular signal is not verified at a destination block as presently claimed.

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[32] Office Action Final, November 5, 2004, page 5, paragraph 8-7.

[33] Office Action Final, November 5, 2004, page 6, first three lines.

[34] Office Action Final, November 5, 2004, page 6, paragraph 8-10.

Furthermore, the Examiner merely argues, "discard this circuit, section 3, paragraph 1".[35] The phrase "discard this circuit" does not appear to anticipate a step of disabling processing of a particular one of a plurality of attributed signals if a particular signal is not verified at a destination block as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 6 should be reversed.

11. Claim 11 is fully patentable over Tabatabaei

Claim 11 depends from claim 9 and thus contains all of the limitations of claim 9. Consequently, the arguments presented above in support of the patentability of claim 9 are incorporated hereunder in support of claim 11.

Claim 11 further provides a step for verifying a model of a destination block configured to receive at least one of a plurality of attributed signals. Despite the assertion by the Examiner,[36] Tabatabaei appears to be silent regarding verifying a model of a destination block configured to receive at least one of a plurality of attributed signals. Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying a model of a destination block configured to receive at least one of a plurality of attributed signals as presently claimed. As such, claim 11 is fully patentable over the cited reference and the rejection should be withdrawn.

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[35] Office Action Final, November 5, 2004, page 6, paragraph 8-10.

[36] Office Action Final, November 5, 2004, page 6, paragraph 8-11.

12. Claim 21 is fully patentable over Tabatabaei

Claim 21 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 21.

Claim 21 further provides that each of the digital signatures comprise a plurality of pulses. Despite the assertion by the Examiner,[37] Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature) comprising a plurality of pulses. Therefore, Tabatabaei does not appear to disclose or suggest each of one or more digital signatures comprising a plurality of pulses as presently claimed.

Furthermore, the Examiner merely argues "n-bit N, Figure 1".[38] The words "n-bit N" do not appear to anticipate each of one or more digital signatures comprising a plurality of pulses as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 21 should be reversed.

13. Claim 22 is fully patentable over Tabatabaei

Claim 22 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 22.

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[37] Office Action Final, November 5, 2004, page 6, paragraph 8-12.

[38] Office Action Final, November 5, 2004, page 6, paragraph 8-12.

Claim 22 further provides that each of the digital signatures comprise a varying frequency signal. Despite the assertion by the Examiner,[39] the first paragraph of section 3 in Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature) comprising a varying frequency signal. Therefore, Tabatabaei does not appear to disclose or suggest each of one or more digital signatures comprising a varying frequency signal as presently claimed.

Furthermore, the Examiner merely argues "different frequency, section 3, paragraph 1".[40] The phrase "different frequency" does not appear to anticipate each of one or more digital signatures comprising a varying frequency signal as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 22 should be withdrawn.

14. Claim 24 is fully patentable over Tabatabaei

Claim 24 depends from claim 23 and thus contains all of the limitations of claim 23. Consequently, the arguments presented above in support of the patentability of claim 23 are incorporated hereunder in support of claim 24.

Claim 24 further provides that a source for a plurality of signals (connected to a simulator) comprises an analog source block. Despite the assertion by the Examiner,[41] Tabatabaei

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[39] Office Action Final, November 5, 2004, page 6, paragraph 8-13.

[40] Office Action Final, November 5, 2004, page 6, paragraph 8-13.

[41] Office Action Final, November 5, 2004, page 7, paragraph 8-15.

appears to be silent regarding a block CUT (source of the signal I_{DD} - asserted similar to one of the claimed analog signals) being a source for a plurality of signals. Therefore, Tabatabaei does not appear to disclose or suggest that a source for a plurality of signals comprises an analog source block as presently claimed.

Furthermore, Tabatabaei appears to be silent regarding the block CUT being connected to a simulator as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations.

Furthermore, Tabatabaei appears to be silent regarding the block CUT being an analog source block. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 24 should be withdrawn.

15. Claim 25 is fully patentable over Tabatabaei

Claim 25 depends from claim 24 and thus contains all of the limitations of claim 24. Consequently, the arguments presented above in support of the patentability of claim 24 are incorporated hereunder in support of claim 25.

Claim 25 further provides that the source block comprises an adder block. Despite the assertion by the Examiner,[42] Tabatabaei appears to be silent regarding a Built-In Current Monitor (BICM) block being similar to an adder block. Therefore, Tabatabaei does not appear to disclose or suggest a source block comprising an adder block as presently claimed.

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[42] Office Action Final, November 5, 2004, page 7, paragraph 8-16.

Furthermore, the Examiner merely argues "BICI, Figure 1".[43] The acronym "BICI" does not appear to anticipate a source block comprising an adder block as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 25 should be reversed.

16. Claim 26 is fully patentable over Tabatabaei

Claim 26 depends from claim 25 and thus contains all of the limitations of claim 25. Consequently, the arguments presented above in support of the patentability of claim 25 are incorporated hereunder in support of claim 26.

Claim 26 further provides that the source block comprises a digital source block. Despite the assertion by the Examiner,[44] Tabatabaei appears to be silent that the source of the signal I_{DD} (asserted similar to the claimed analog signal) comprises an FF1 (asserted similar to the claimed digital source block). Therefore, Tabatabaei does not appear to disclose or suggest a source block comprising a digital source block as presently claimed. As such, claim 26 is fully patentable over the cited reference and the rejection should be withdrawn.

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[43] Office Action Final, November 5, 2004, page 7, paragraph 8-16.

[44] Office Action Final, November 5, 2004, page 7, paragraph 8-17.

17. Claim 27 is fully patentable over Tabatabaei

Claim 27 depends from claim 23 and thus contains all of the limitations of claim 23. Consequently, the arguments presented above in support of the patentability of claim 23 are incorporated hereunder in support of claim 27.

Claim 27 further provides that the digital signatures comprise a plurality of pulses. Despite the assertion by the Examiner,[45] Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature) comprising a plurality of pulses. Therefore, Tabatabaei does not appear to disclose or suggest one or more digital signatures comprising a plurality of pulses as presently claimed.

Furthermore, the Examiner merely argues "n-bit N, Figure 1".[46] The words "n-bit N" do not appear to anticipate one or more digital signatures comprising a plurality of pulses as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 27 should be reversed.

18. Claim 28 is fully patentable over Tabatabaei

Claim 28 depends from claim 27 and thus contains all of the limitations of claim 27. Consequently, the arguments presented above in support of the patentability of claim 27 are incorporated hereunder in support of claim 28.

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[45] Office Action Final, November 5, 2004, page 7, paragraph 8-18.

[46] Office Action Final, November 5, 2004, page 7, paragraph 8-18.

Claim 28 further provides that the plurality of pulses have a unique width to identify an analog signal. Despite the assertion by the Examiner,[47] Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature) as a plurality of pulses having a unique width. Therefore, Tabatabaei does not appear to disclose or suggest a plurality of pulses having a unique width to identify an analog signal as presently claimed.

Furthermore, the Examiner merely argues "n-bit N, Figure 1".[48] The words "n-bit N" do not appear to anticipate a plurality of pulses having a unique width to identify an analog signal as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 28 should be reversed.

19. Claim 29 is fully patentable over Tabatabaei

Claim 29 depends from claim 27 and thus contains all of the limitations of claim 27. Consequently, the arguments presented above in support of the patentability of claim 27 are incorporated hereunder in support of claim 29.

Claim 29 further provides that the digital signatures comprise a varying frequency signal. Despite the assertion by the Examiner,[49] the first paragraph of section 3 in Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signature)

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[47] Office Action Final, November 5, 2004, page 7, paragraph 8-19.

[48] Office Action Final, November 5, 2004, page 7, paragraph 8-19.

[49] Office Action Final, November 5, 2004, page 7, paragraph 8-20.

comprising a varying frequency signal. Therefore, Tabatabaei does not appear to disclose or suggest one or more digital signatures comprising a varying frequency signal as presently claimed.

Furthermore, the Examiner merely argues "different frequency, section 3, paragraph 1".[50] The phrase "different frequency" does not appear to anticipate one or more digital signatures comprising a varying frequency signal as presently claimed. Therefore, *prima facie* anticipation has not been established for lack of evidence that the reference discloses or suggests all of the claim limitations. As such, the rejection of claim 29 should be withdrawn.

C. CONCLUSION

The cited reference does not disclose or suggest (i) a step for generating one or more source signals by adding a digital signature to each of one or more analog signals, (ii) a step for generating one or more attributed signals each having a unique digital signature and (iii) a source for a plurality of signals and a simulator connected to the source as recited in claims 1, 9 and 23, respectively. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending

[50] Office Action Final, November 5, 2004, page 7, paragraph 8-20.

claims, and hold that the claims are not rendered obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 9, and/or 23 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable claims.

Respectfully submitted,

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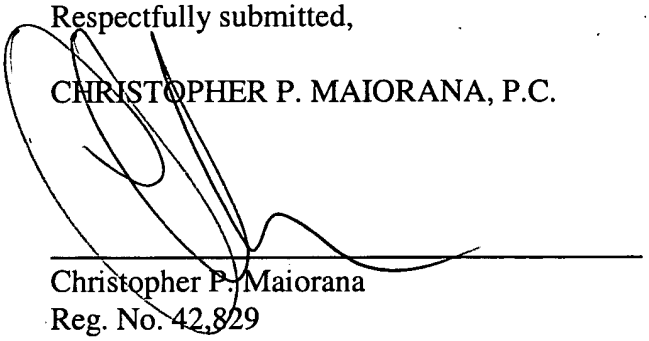

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VIII. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. A method for verification, comprising the steps of:

(A) generating one or more analog signals utilized by an analog design;

(B) generating one or more source signals by adding a digital signature to each of said analog signals; and

(C) modeling said analog design using said source signals in place of said analog signals for verifying connectivity.

2. The method according to claim 1, wherein step (C) further comprises the step of:

performing one or more simulations of said analog design with said source signals propagating through said analog design.

3. The method according to claim 1, wherein each of said digital signatures corresponds to a type of said analog signals having a predetermined parameter.

4. The method according to claim 1, wherein each of said digital signatures comprises a unique pulse width.

5. The method according to claim 1, further comprising the step of:

performing verification of said analog design.

6. The method according to claim 2, wherein performing said simulations further comprises the sub-step of:

verifying a connectivity of said analog signals through said analog design.

7. The method according to claim 2, wherein performing said simulations further comprises the sub-step of:

verifying a model of an analog block within said analog design configured to receive at least a particular one of said analog signals.

8. The method according to claim 7, wherein verifying said model further comprises the sub-step of:

verifying an output signal of said analog block for said digital signature associated with said particular one of said analog signals.

9. A method for testing a model of an analog device, comprising the steps of:

(A) generating one or more attributed signals each (i) having a unique digital signature and (ii) presented by a source block within said model of said analog device; and

(B) verifying connectivity of said attributed signals to a destination block within said model of said analog device by verifying reception of said unique digital signatures associated with each of said attributed signals at said destination block.

10. The method according to claim 9, further comprising the step of:

disabling processing of a particular one of said attributed signals if said particular signal is not verified at said destination block.

11. The method according to claim 9, further comprising the step of:

verifying a model of said destination block configured to receive at least one of said attributed signals.

12. (CANCELED)

13. (CANCELED)

14. (CANCELED)

15. (CANCELED)

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)

21. The method according to claim 1, wherein each of said digital signatures comprises a plurality of pulses.

22. The method according to claim 1, wherein each of said digital signatures comprises a varying frequency signal.

23. A system comprising:

a source for a plurality of signals, at least one of said signals representing an analog signal having a digital signature; and

a simulator connected to said source and configured to (i) simulate an analog design, (ii) receive said signals and (iii) verify a connectivity of said analog signal in said analog design using said digital signature.

24. The system according to claim 23, wherein said source comprises an analog source block configured to generate said analog signal.

25. The system according to claim 24, wherein said source further comprises an adder block configured to (i) generate said digital signature and (ii) add said digital signature to said analog signal.

26. The system according to claim 25, wherein said source further comprises a digital source block configured to generate at least one of said signals representing a digital signal.

27. The system according to claim 23, wherein said digital signature comprises a plurality of pulses.

28. The system according to claim 27, wherein said pulses have a unique width to identify said analog signal.

29. The system according to claim 27, wherein said digital signature has a varying frequency.